RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. THIRD SEMESTER EXAMINATION, MARCH 2022

SECOND YEAR [BATCH 2020-23]

Date : 02/03/2022 **PHYSICS (HONOURS)**

Time : 11 am – 1 pm **Paper : V [CC5]** Full Marks : 50

Answer **any five** questions of the following: [5×10]

1. a) How energy bond forms in solid.

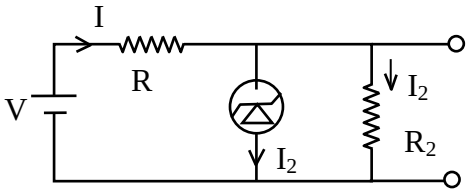
   b) How energy bond bend in a p-n junction semiconductor and show its Fermi level. What is depletion layer for p-n diode? [5+5]

2. a) What is load line for p-n diode?

   b) How static characteristics of a diode is different from dynamic characteristics of the diode?

   c) Compare the ripple factor of a full wave rectifier to a half wave rectifier.

   d)



   Where, V = 15 volt.

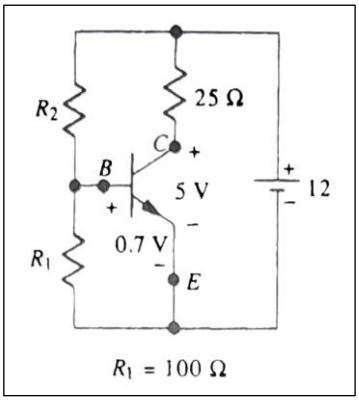
   The 13 volt, 0.39 terner diode. operates at minimum diode current of 2mA.

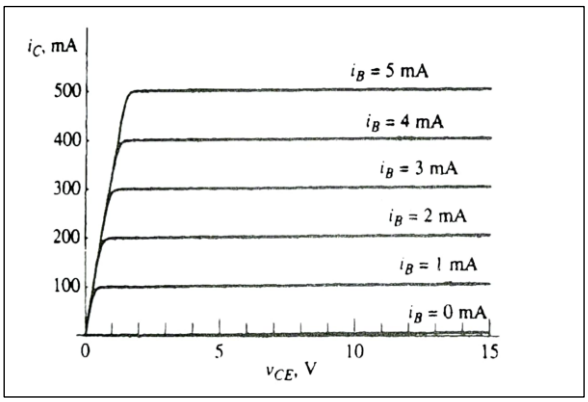
   In the circuit R = 100 Ω , R_2 = 1 KΩ . Determine the limits between which the supply voltage V can vary without loss of regulation. [2+2+3+3]

3. a) Is the input characteristics of a BJT in CE configuration similar to that of a resistor, a *pn* junction diode or an open circuit? Explain in brief. In the saturation region, does the transistor act as a switch that is ON or OFF? [2+1]

   b) 'The load-line intersects the current axis at the current that would flow if the BJT were replaced by a short circuit' – Is this statement true or false? Explain. To be used as an amplifier, the transistor must be biased into its cut-off, active, breakdown, ohmic or saturation region? [2+1]

   c) A transistor circuit is shown in the following with its output characteristics. Determine R2 to make the collector-emitter voltage +5 V, as shown in the circuit. [4]

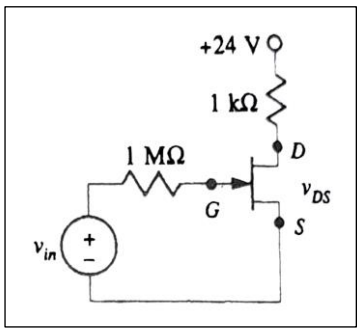


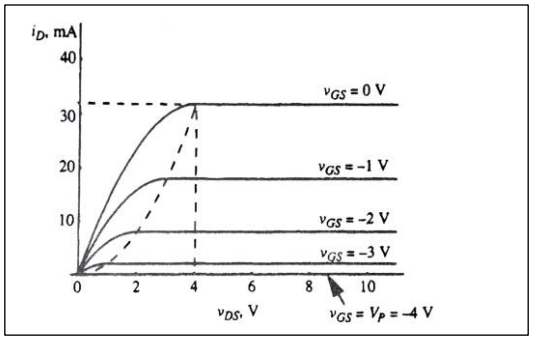


4. a) Why is the channel shown as a dashed line for the enhancement type MOSFET, yet shown as a solid line for the depletion type MOSFET? Explain, if it is possible to use a depletion type MOSFET as enhancement type MOSFET or not and vice-versa. [1+2]

b) An NMOS has a threshold voltage of –3 Volt. Is this a depletion or enhancement mode MOSFET? Explain. What is CMOS? Design an AND gate using CMOS circuits. [1+1+2]

c) The JFET in the following figure has I_{DSat} = 32 mA and V_P = –4 Volt, and hence the output characteristics shown below also. Assume that the FET is in the saturation region throughout this problem. Find i_D to give v_{DS} = 12 Volt; also determine v_{in} which gives v_{DS} = 12 Volt. [3]

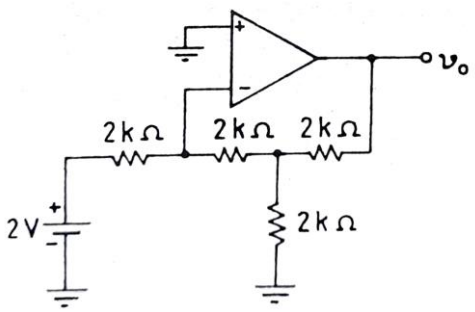




5. a) For a Voltage gain of +5 Volt in an OPAMP amplifier circuit, the feedback comes from the output to which input terminal? Which input terminal gets the input signal? [1+1]

b) What operation is performed in an inverting amplifier if the feedback resistor is replaced by a capacitor or by a diode, respectively? If an OPAMP has ±10 Volt as the power supply source and a gain of 80 dB, at what value of $v_+ - v_-$ does the OPAMP saturate? [2+2]

c) In the following figure the OPAMP is activated using a ±10 Volt power supply source. Determine the value of output voltage for the given circuit. Also mention what should be the output voltage if all the resistances are replaced by 1KΩ resistors. [4]



6. a) What are the advantages of using crystal oscillator over Hartley and Colpitts oscillator for generating RF oscillations? Why are audio frequencies (AF) and very high frequencies (VHF) not possible to generate using piezoelectric crystals? [2+1]

b) It is found that using negative feedback the band-width (BW) of an amplifier increases significantly. Show that the product of Gain and BW remains same after feeding the amplifier with negative feedback. [3]

c) A Wien bridge oscillator is to be operated in the frequency range 20 Hz to 20 KHz. The variable capacitances have a range of 100 pF to 1000 pF. Find the resistance values required. If the resistances in the other arms are in the 5:1, find out the gain of the amplifier. [4]

7. a) Which mode among CB, CE and CC is suitable for the use in multistage amplifier and why? Compare class A, B, C and AB amplifiers with respect to their power efficiencies. [2+2]

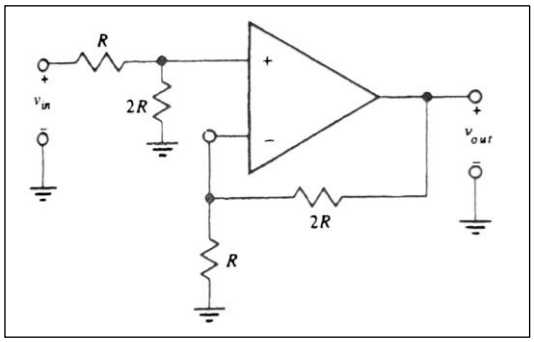
b) Four identical amplifying stages are cascaded to form a multistage amplifier. If lower and upper half power frequency of a single stage are 100 Hz and 10 KHz respectively, find their values for the multistage amplifier. [4]

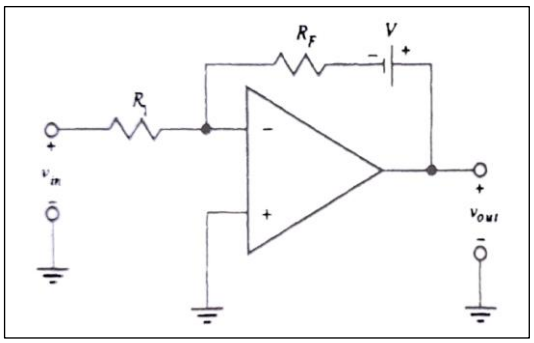
c) A bistable multivibrator has a memory and thus it is capable of storing a single bit. Is this true? Explain your answer. [2]

8. a) Describe how antilog amplifier can be designed using OPAMP. Derive the relation between input and output voltages. [3]

b) In the following figure there is shown a feedback path. Find the value of loop gain and also the gain of the system with the feedback. [3]

c) For the following two OPAMP based circuits find out v_{out}/v_{in} respectively: [2+2]





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